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EXAMINER	
ZARNEKE, DAVID A	
ART UNIT	**PAPER NUMBER**
2891	

DATE MAILED: 06/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/731,453	JOSHI ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2891	

-- The MAILING DATE f this communication appears on the cov r sheet with the c rresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 33-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 33-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The amendment filed 4/3/06 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: the substrate being recited as being a leadframe substrate. The only mention of a leadframe in the specification is with respect to Figure 28, in which the chip scale package of the claim is attached to a leadframe (specification page 15, [0080]). Therefore, the specification fails to teach the substrate of the chip scale package as being a leadframe. Further, the specification (page 7, [0041]) states that the substrate can be made of any known semiconductor substrate. Therefore, it could not be a leadframe.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 15, 19, 37, and 41 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to

reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The amendment now recites the substrate as being a leadframe substrate. The only mention of a leadframe in the specification is with respect to Figure 28, in which the chip scale package of the claim is attached to a leadframe (specification page 15, [0080]). Therefore, the specification fails to teach the substrate of the chip scale package as being a leadframe. Further, the specification (page 7, [0041]) states that the substrate can be made of any known semiconductor substrate. Therefore, it could not be a leadframe.

Response to Arguments

Applicant's argument with respect to the new leadframe limitation of amended claims 1, 15, 19, 37, and 41 have been fully considered but they are not persuasive. See the 112 new matter rejection above. Therefore, the new matter is not considered and the previous rejection stands as written.

Applicant's arguments with respect to the new conductive particle limitation of amended claims 11, 15, 19, 33, and 41 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 7, 10, 37-38 and 40 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Higashi et al., US Patent 5,918,113 (figures 10a-11).

Regarding claim 2, Higashi teaches at least one conductive particle is located between the stud bump and the bond pad (Figure 10b).

With respect to claim 3, Higashi teaches the conductive particles comprise metal with an insulating layer (3, 49+).

As to claims 4 and 38, Higashi teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (3, 49+).

In re claim 5, Higashi inherently teaches the chip contains an integrated circuit in communication with a chip pad (the bump [54] electrically connects to the integrated circuit).

Regarding claims 7 and 40, Higashi teaches the chip does not contain solder paste (figures).

With respect to claim 10, Higashi teaches the chip does not contain a chip pad overlying an integrated circuit (figures).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

> the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higashi et al., US Patent 5,918,113 (figures 10a-11), as applied to claim 1 above, and further in view of Applicant's admitted prior art (APA) Figures 1-3.

Higashi fails to teach the chip contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

APA Figures 1-3 teaches a chip that contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a chip that contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern of APA in the invention of Higashi because RDL patterns allow for greater flexibility and to take advantage of unused chip space.

Claim 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashi et al., US Patent 5,918,113 (figures 10a-11), as applied to claim 1 above.

Regarding claim 8, Higashi, which teaches the use of a gold (Au) stud bump [54], fails to teach the stud bump comprises Cu.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the a Cu stud bump in place of the Au stud bump of Higashi because Cu and Au are conventionally known in the art equivalent metals known to be used as stud bumps. One would be motivated to substitute Cu for Au because Cu is cheaper than Au.

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

With respect to claim 9, while Higashi fails to teach the stud bump is a coined stud bump, (1) It would have been obvious to one ordinary skill in the art at the time of the invention to optimize the method of forming the stud bump (MPEP 2144.05); and (2) the manner in which it is formed is irrelevant in a product claim since product by process

limitations are not given patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Claims 11, 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashi et al., US Patent 5,918,113 (figures 10a-11), in view of Nishida et al., US Patent 6,926,796, and/or Kaneda et al., US Patent 6,223,429.

Higashi teaches a wafer-level chip scale package, comprising:

a chip [50] containing a stud bump [54];

a substrate [10] containing a bond pad [12a]; and

an adhesive material [20] containing conductive particles located between the chip and the substrate with at least one conductive particle located between the stud bump and the bond pad (figure 10c).

Higashi, which teaches the use of a gold (Au) stud bump [54], fails to teach the stud bump comprises Cu.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the a Cu stud bump in place of the Au stud bump of Higashi because Cu and Au are conventionally known in the art equivalent metals known to be used as

stud bumps. One would be motivated to substitute Cu for Au because Cu is cheaper than Au.

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Higashi further fails to teach the conductive particles as comprising a metal and an insulating layer.

Nishida (Figure 1G & 19, 4-43) and Kaneda (6, 35+) both teach the use of conductive particles comprising a metal and an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles comprising a metal and an insulating layer of in the invention of Higashi because Kaneda teaches this type of conductive particle improves the insulating properties in the lateral direction (6, 35+).

As to claim 12, Higashi teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (3, 49+).

Regarding claim 14, Higashi teaches the chip does not contain solder paste (figures).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higashi et al., US Patent 5,918,113 (figures 10a-11), in view of Nishida et al., US Patent

6,926,796, and/or Kaneda et al., US Patent 6,223,429, as applied to claim 11 above, and further in view of Applicant's admitted prior art (APA) Figures 1-3.

Higashi fails to teach the chip contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

APA Figures 1-3 teaches a chip that contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a chip that contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern of APA in the invention of Higashi because RDL patterns allow for greater flexibility and to take advantage of unused chip space.

Claims 15, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashi et al., US Patent 5,918,113 (figures 10a-11), in view of Nishida et al., US Patent 6,926,796, and/or Kaneda et al., US Patent 6,223,429.

Higashi teaches a packaged semiconductor device, comprising:

a chip [50] containing a stud bump [54];

a substrate [10] containing a bond pad [12a]; and

an adhesive material [20] containing conductive particles located between the chip and the substrate with at least one conductive particle located between the stud bump and the bond pad (figure 10c).

Higashi, which teaches the use of a gold (Au) stud bump [54], fails to teach the stud bump comprises Cu.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the a Cu stud bump in place of the Au stud bump of Higashi because Cu and Au are conventionally known in the art equivalent metals known to be used as stud bumps. One would be motivated to substitute Cu for Au because Cu is cheaper than Au.

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

Higashi further fails to teach the conductive particles as comprising a metal and an insulating layer.

Nishida (Figure 1G & 19, 4-43) and Kaneda (6, 35+) both teach the use of conductive particles comprising a metal and an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles comprising a metal and an insulating layer of in the invention of Higashi because Kaneda teaches this type of conductive particle improves the insulating properties in the lateral direction (6, 35+).

As to claim 16, Higashi teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (3, 49+).

Regarding claim 18, Higashi teaches the chip does not contain solder paste (figures).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higashi et al., US Patent 5,918,113 (figures 10a-11), in view of Nishida et al., US Patent 6,926,796, and/or Kaneda et al., US Patent 6,223,429, as applied to claim 15 above, and further in view of Applicant's admitted prior art (APA) Figures 1-3.

Higashi fails to teach the chip contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

APA Figures 1-3 teaches a chip that contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a chip that contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern of APA in the invention of Higashi because RDL patterns allow for greater flexibility and to take advantage of unused chip space.

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higashi et al., US Patent 5,918,113 (figures 10a-11), in view of Nishida et al., US Patent 6,926,796, and/or Kaneda et al., US Patent 6,223,429.

Higashi teaches a packaged semiconductor device, comprising:

a chip [50] containing a stud bump [54];

a substrate [10] containing a bond pad [12a]; and

an adhesive material [20] containing conductive particles contacting both the chip and the substrate (figure 10c).

Higashi fails to teach the conductive particles as comprising a metal and an insulating layer.

Nishida (Figure 1G & 19, 4-43) and Kaneda (6, 35+) both teach the use of conductive particles comprising a metal and an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles comprising a metal and an insulating layer of in the invention of Higashi because Kaneda teaches this type of conductive particle improves the insulating properties in the lateral direction (6, 35+).

Claims 33, 34, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashi et al., US Patent 5,918,113 (figures 10a-11), in view of Nishida et al., US Patent 6,926,796, and/or Kaneda et al., US Patent 6,223,429.

Higashi teaches a packaged semiconductor device, comprising:

a chip [50] containing a stud bump [54];

a substrate [10] containing a bond pad [12a]; and

an adhesive material [20] containing conductive particles located between the chip and the substrate (figure 10c).

Higashi fails to teach the conductive particles as comprising a metal and an insulating layer.

Nishida (Figure 1G & 19, 4-43) and Kaneda (6, 35+) both teach the use of conductive particles comprising a metal and an insulating layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles comprising a metal and an insulating layer of

in the invention of Higashi because Kaneda teaches this type of conductive particle improves the insulating properties in the lateral direction (6, 35+).

As to claim 34, Higashi teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (3, 49+).

Regarding claim 36, Higashi teaches the chip does not contain solder paste (figures).

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higashi et al., US Patent 5,918,113 (figures 10a-11), in view of Nishida et al., US Patent 6,926,796, and/or Kaneda et al., US Patent 6,223,429, as applied to claim 33 above, and further in view of Applicant's admitted prior art (APA) Figures 1-3.

Higashi fails to teach the chip contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

APA Figures 1-3 teaches a chip that contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a chip that contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern of APA in the invention of Higashi because RDL patterns allow for greater flexibility and to take advantage of unused chip space.

Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higashi et al., US Patent 5,918,113 (figures 10a-11), in view of Nishida et al., US Patent

6,926,796, and/or Kaneda et al., US Patent 6,223,429, as applied to claim 37 above, and further in view of Applicant's admitted prior art (APA) Figures 1-3.

Higashi fails to teach the chip contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

APA Figures 1-3 teaches a chip that contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a chip that contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern of APA in the invention of Higashi because RDL patterns allow for greater flexibility and to take advantage of unused chip space.

Claims 41, 42, 44 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashi et al., US Patent 5,918,113 (figures 10a-11), in view of Sawamoto, US Patent 6,426,566, or Ding et al., US Patent 6,737,300, or Shibata, US Patent 6,461,890, and also in view of Nishida et al., US Patent 6,926,796, and/or Kaneda et al., US Patent 6,223,429.

Higashi teaches a wafer-level chip scale package without solder paste, comprising:

a chip [30] containing a stud bump [32];

a substrate [10] containing a bond pad [12a]; and

an adhesive material [20] containing conductive particles located between the chip and the substrate.

Higashi fails to teach conductive particles contact both the stud bump and the bond pad.

Sawamoto, Ding and Shibata all teach conductive particles contact both the stud bump and the bond pad.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the invention of Sawamoto, Ding and Shibata in the invention of Higashi because it is much simpler to apply an adhesive with conductive particles throughout than to align the conductive particles on one side of the adhesive.

Higashi also fails to teach the conductive particles as comprising a metal and an insulating layer.

Nishida (Figure 1G & 19, 4-43) and Kaneda (6, 35+) both teach the use of conductive particles comprising a metal and an insulating layer.
It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive particles comprising a metal and an insulating layer of in the invention of Higashi because Kaneda teaches this type of conductive particle improves the insulating properties in the lateral direction (6, 35+).

As to claim 42, Higashi teaches the adhesive material comprises an anisotropic conductive film, an anisotropic conductive paste, or an isotropic conductive paste (3, 49+).

Regarding claim 44, Higashi, which teaches the use of a gold (Au) stud bump [54], fails to teach the stud bump comprises Cu.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the a Cu stud bump in place of the Au stud bump of Higashi because Cu and Au are conventionally known in the art equivalent metals known to be used as stud bumps. One would be motivated to substitute Cu for Au because Cu is cheaper than Au.

The substitution of one known equivalent technique for another may be obvious even if the prior art does not expressly suggest the substitution (Ex parte Novak 16 USPQ 2d 2041 (BPAI 1989); In re Mostovych 144 USPQ 38 (CCPA 1964); In re Leshin 125 USPQ 416 (CCPA 1960); Graver Tank & Manufacturing Co. V. Linde Air Products Co. 85 USPQ 328 (USSC 1950).

With respect to claim 45, while Higashi fails to teach the stud bump is a coined stud bump, (1) It would have been obvious to one ordinary skill in the art at the time of the invention to optimize the method of forming the stud bump (MPEP 2144.05); and (2) the manner in which it is formed is irrelevant in a product claim since product by process limitations are not given patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

Claim 43 is rejected under 35 U.S.C. 103(a) as being unpatentable over Higashi et al., US Patent 5,918,113 (figures 10a-11), in view of Sawamoto, US Patent 6,426,566, or Ding et al., US Patent 6,737,300, or Shibata, US Patent 6,461,890, also in view of Nishida et al., US Patent 6,926,796, and/or Kaneda et al., US Patent 6,223,429, as applied to claim 41 above, and further in view of Applicant's admitted prior art (APA) Figures 1-3.

Higashi, Sawamoto, Ding and Shibata all fail to teach the chip contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

APA Figures 1-3 teaches a chip that contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a chip that contains a re-distributed line pattern and an insulating layer covering a portion of the RDL pattern of APA in the invention of Higashi because RDL patterns allow for greater flexibility and to take advantage of unused chip space.

Conclusion

Any inquiry concerning this communication from the examiner should be directed to David A. Zarneke at (571)-272-1937. The examiner can normally be reached on M-Th 7:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1722. The fax phone number where this application is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David A. Zarneke
Primary Examiner
June 6, 2006